Real-Time Power Electronics Simulation

Advanced Electrical Power System Thrust Science & Technology Review & Workshop

November 5-7, 2002

McLeod Institute of Simulation Sciences
California State University, Chico

Participants

- **ONR**
  - Terry Ericsen
- **CSU, Chico**
  - Roy Crosbie, Professor and co-PI
  - John Zenor, Professor and co-PI
  - Dale Word, Professor
  - Dick Bednar, Professor
  - Ralph Hilzer, Research Professor
  - Nari Hingorani, Consultant
  - **CSU Chico Students**: Jey, Ruban, Rajeev, Zarak, Swaroop, Purti, Manisha

Project Goals

- Real-time simulation of power electronic systems with frame times of less than 10 μsec
- Integration with VTB/VXE
- Hardware in the loop simulation
- Low cost using PC and commercially available DSP Boards

Basic Approach

- Arrays of digital signal processors form simulation engine
- Commercial 4-processor board plugs into PCI bus of PC
- A/D D/A mezzanine board
- D/D Link Port connection to external DSP Boards or Simulator
- Coding in C++
- VTB/VXE runs on PC host

Simulation Platforms

- **PC only**
  - Used for initial development and demonstrations and non-real time simulation.

- **PC with Plugged in DSP Board**

  Bittware 4*AD21160 processor PCI board
  - 80 MHz processors
  - 66 MHz 64-bit PCI bus
  - 8*A/D, 4*D/A, 16-bit, 100kHz, simultaneous sampling

  PC with Univ. of South Carolina's VTB/VXE use for all man/machine interface and data plotting

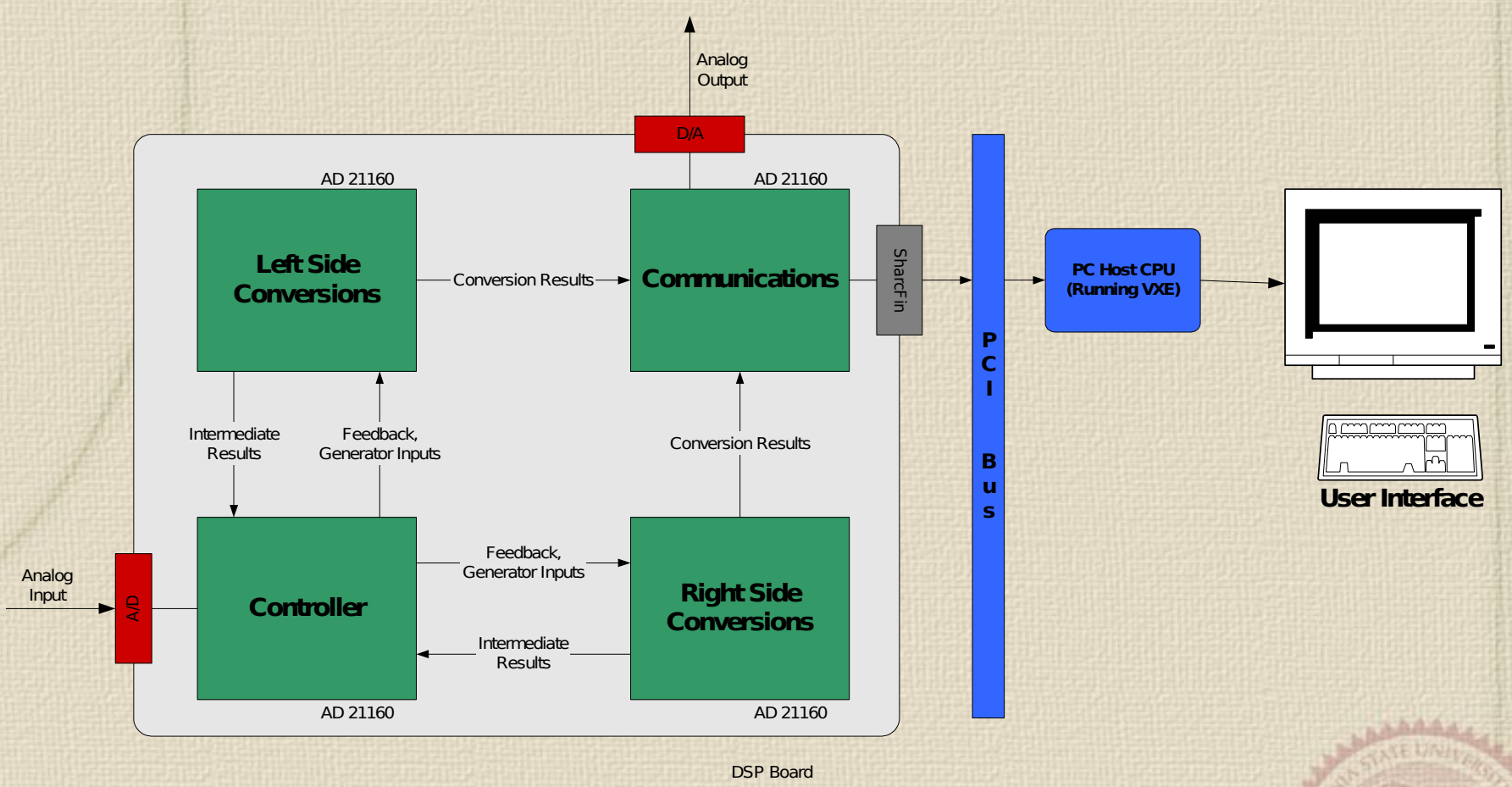
VTB/VXE Interface

- Parameter entry and control of execution and output through VTB interfaces
- Output graphing uses VXE
- DSP models give windowed data with time reference
- Parameter changes during execution

DSP Communication Techniques

- Detailed investigation of DSP data transfer mechanisms
- Timing studies to determine most efficient method
- Synchronization of data transfers with current time-step

DSP Communications Architecture



Current Models *(PC and DSP Versions)*

- 6-pulse, back-to-back without filters
- 6-pulse, back-to-back with R-C filters
- 6-pulse, 3-level back-to-back with R-C filters
- 12-pulse, 2-level, back-to-back with R-C filters

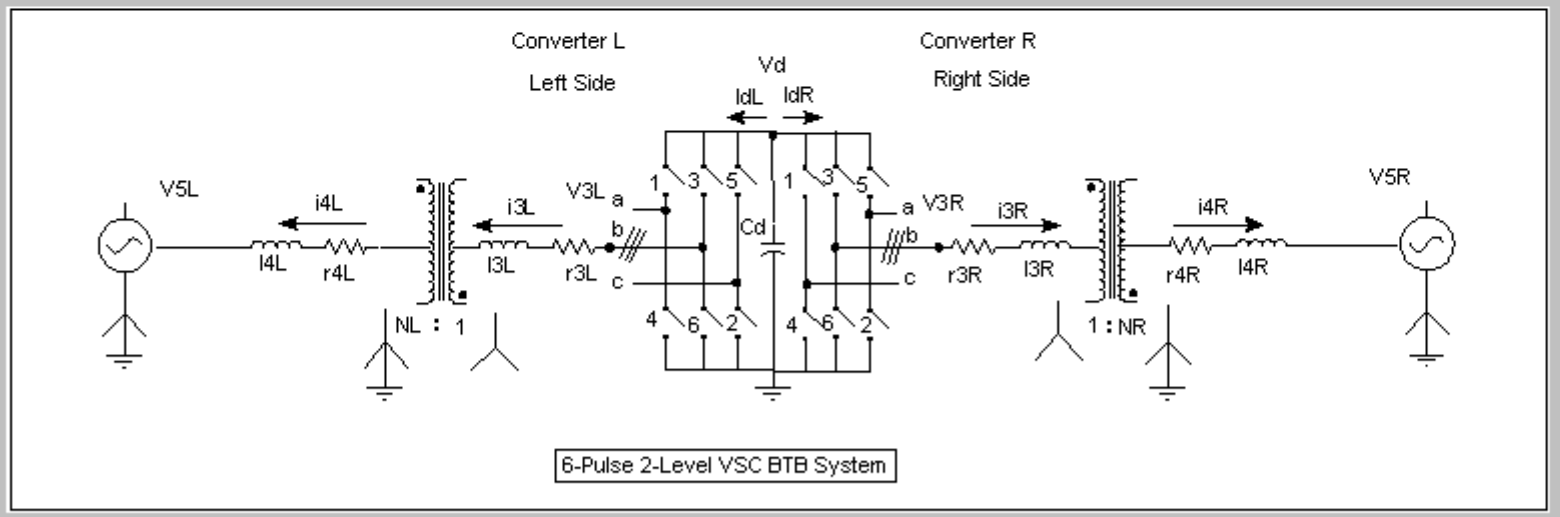
Parameter Values

Name : 6PVSCBTBDSPWoF0

Description : 6 Pulse Voltage Sourced Conver

Parameter	Values	Units
interval	10.000	Unitless
Vd	0.00000	volt
C	0.20000	farads
Vd_slopecount	500.00	Unitless
RLcontrol	1.0000	Unitless
Vdset	1.0000	volt
Idset	1.0000	ampere
gen_ampliR	0.45000	volt
freqR	60.000	Hz
phiR	0.00000	degrees
tri_ampliR	1.1000	P.U
r3R	10.0000m	ohms
r4R	15.000m	ohms

Circuit Diagram :



OK

Cancel

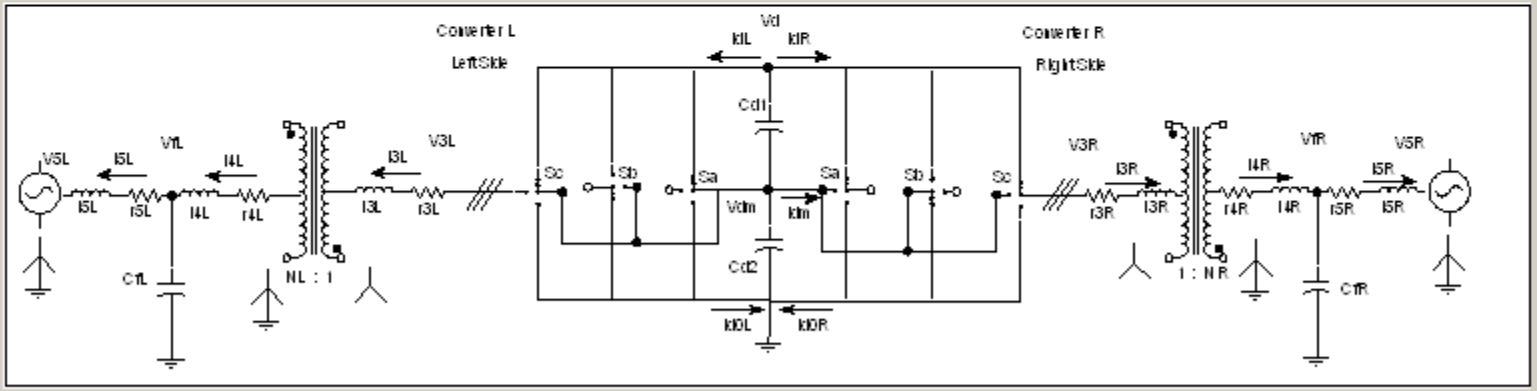
Parameter Values

Name : DSP_6P3LVSCBTBoFXpwm0

Description : 6 Pulse Voltage Sourced Conver

Parameter	Values	Units
Vd	.8	volt
Vdm	.4	volt
C1	0.40000	farads
C2	0.40000	farads
CfL	3.0000m	farads
CfR	3.0000m	farads
rhoL	0.00000	degree
rhoR	26.000	degree
RLcontrol	1.0000	Unitless
Vdset	1.2000	volt
Idset	1.0000	ampere
gen_ampliL	0.60000	volt
gen_ampliR	0.50000	volt

Circuit Diagram :



OK Cancel

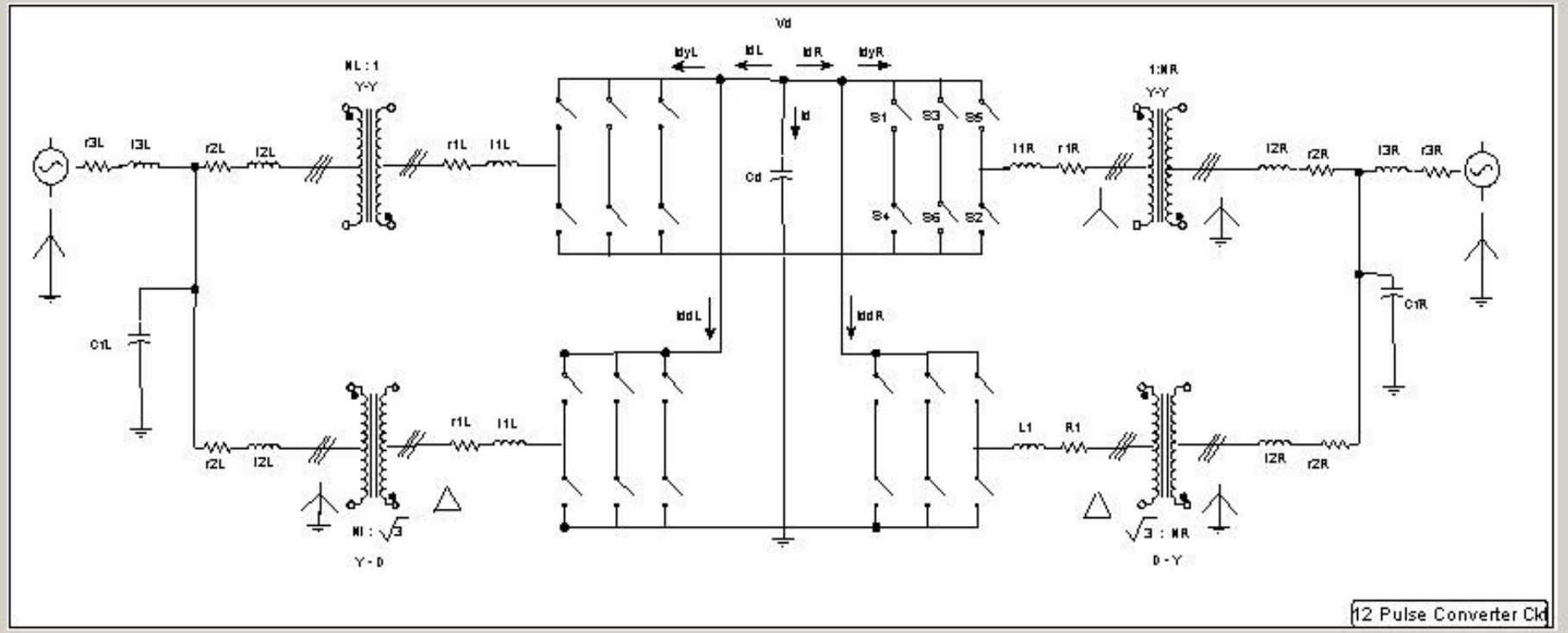
Parameter Values

Name : 12PVSCBTBwFXpwm28643312

Description : 12 Pulse Voltage Sourced Conv

Parameter	Values	Units
Vd	0.80000	volt
C	0.20000	farads
Cf_L	1.0000m	farads
Cf_R	1.0000m	farads
RLcontrol	1.0000	Unitles:
Vdset	1.2000	volt
Idset	1.0000	ampere
gen_ampli_L	0.60000	volt
gen_ampli_R	0.45000	volt
freq_L	60.000	Hz

Circuit Diagram :



OK

Cancel

Design Criteria for VTB Integration

- **DSP-based models must run in real time**
  - Graphical output and user-interface must not affect model timing
  - Models should run continuously, without interruption by PC
- **Non real-time, PC-only models are also required**
  - Readily available environment for testing and development
  - Two models should give identical results
  - Input data files and user interface as identical as practical
- **Maintain look and feel of VTB/VXE environment**
- **Ability to interface to external hardware**

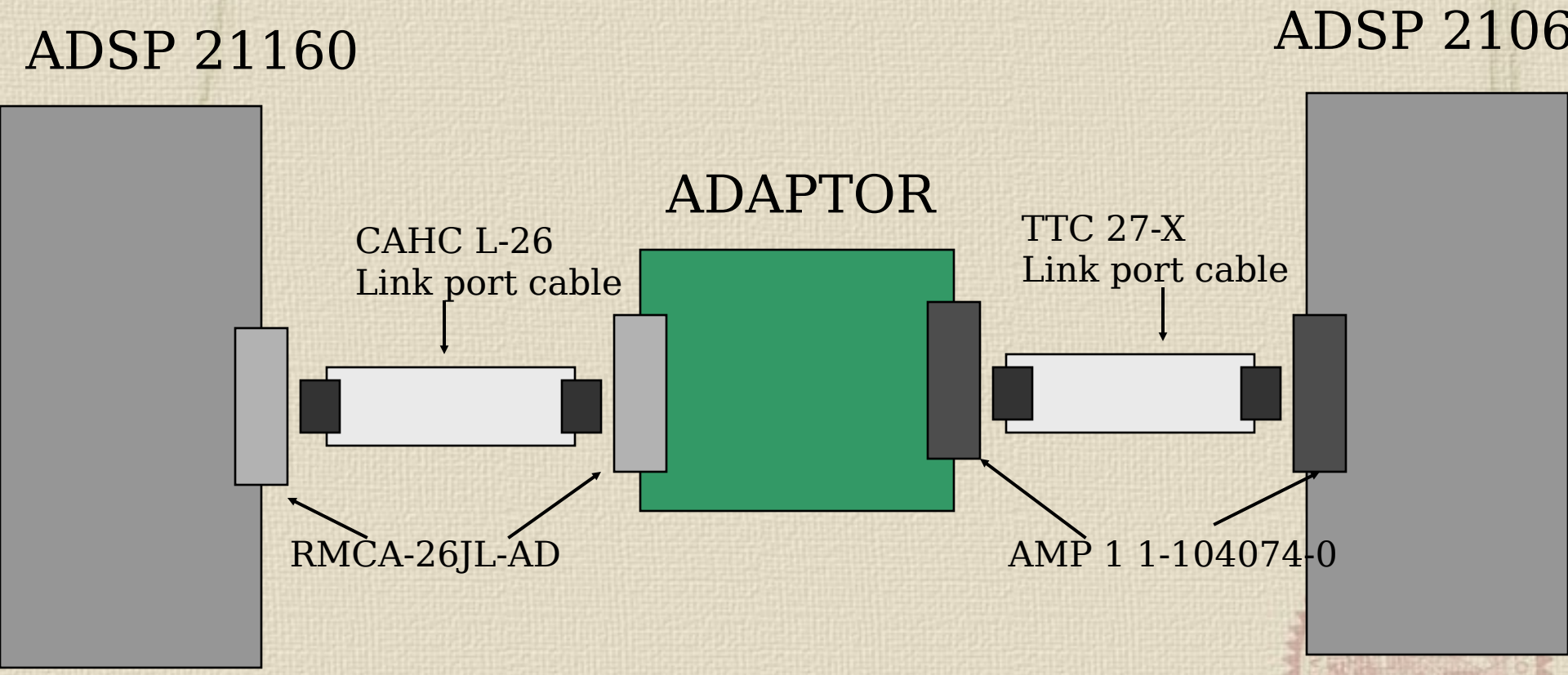
Integration Time Steps Required

- Experimental investigations with current models indicate that for good accuracy, the following maximum integration steps will be required for PWM control:
  - 10 µsec for 1kHz PWM (15*line frequency)
  - 6 µsec for 2 kHz PWM (33*line frequency)
  - 3 µsec for 20 kHz PWM (333*line frequency)

MinimumTime Step Achieved (DSP Versions)

- 6-pulse, back-to-back without filters
  5 us
- 6-pulse, back-to-back with R-C filters
  6.5 us
- 6-pulse, 3-level back-to-back with R-C filters
  8 us
- 12-pulse, 2-level, back-to-back with R-C filters

D/D Hardware in the Loop



Summary of Project Goals

- Low-cost commercially available PC based and plugin DSP Boards simulation
- Greatest feasible integration with VTB
- Implement complete model sets with maximum 10 μsec frame times
- Reduce frame times to support 20kHz PWM models
- Implement real-time model of reconfiguration scenario
- Implement models with D/D and A/D - D/A hardware in the loop